Journal of Engineering Research and Reports

14(2): 15-19, 2020; Article no.JERR.58701
ISSN: 2582-2926

Bond Line Thickness Characterization for QFN Package Robustness

Bryan Christian S. Bacquian[1*], Edwin M. Graycochea Jr[1], Frederick Ray I. Gomez[1] and Rennier S. Rodriguez[1]

[1]New Product Development & Introduction, STMicroelectronics, Inc., Calamba City, Laguna, 4027, Philippines.

Authors' contributions

This work was carried out in collaboration amongst the authors. All authors read, reviewed and approved the final manuscript.

Article Information

DOI: 10.9734/JERR/2020/v14i217119
Editor(s):
(1) Dr. Leandro A. Pasa, Federal University of Technology Paraná, Brazil.
Reviewers:
(1) I. Rexiline Sheeba, Sathyabama Institute of Science and Technology, India.
(2) G. Mary Valantina, Sathyabama Institute of Science and Technology, India.
Complete Peer review History: http://www.sdiarticle4.com/review-history/58701

Original Research Article

Received 22 April 2020
Accepted 29 June 2020
Published 06 July 2020

ABSTRACT

The paper focused on the evaluation of quad-flat no-leads (QFN) semiconductor package with small silicon die on different machine platforms to achieve a higher bond line thickness (BLT) of greater than 30 µm. The characterization or evaluation was narrowed down into two main diebonding machines with the objective of attaining a higher BLT for small die. High BLT capability is desired to generate clearance for the shrinkage of the glue, henceforth mitigating the glue voids. Diebond Machine 2 was able to achieve the target BLT with 30.89 µm average compared to 18.25 µm for Machine 1. Moreover, the target BLT range could only be achieved in Machine 2 only. For future works, the machine and configuration could be used for devices with comparable requirement.

Keywords: QFN; diebond process; glue; BLT.

**Corresponding author: Email: bryan-christian.bacquian@st.com;*

1. INTRODUCTION

Semiconductor packaging technologies such as the tapeless quad-flat no-leads (QFN) leadframe technology are continuously developed and improved to produce high quality and robust products for various applications. Common direction of semiconductor manufacturing companies is to increase the production yields and maintain high quality while minimizing the wastage and assembly rejections. In this paper, a semiconductor QFN package is determined to be critical due to the high occurrence of glue voids as seen in Fig. 1. Voids or gaps inside the adhesion material particularly the glue is created before and/or after the diebonding process cycle.

The suggested solution on this issue is to evaluate and characterize a higher target bond line thickness (BLT) for small die to create clearance for the shrinkage of the glue. The clearance is computed from the measurement of the shrinkage rate of the glue or the average difference in BLT between "wet" and cured glue. In this study, the shrinkage of the highly conductive glue is measured with an average of 4.1 µm with 1.98 sigma. The targeted BLT in this study is greater than 30 µm with reference to the spacer's average diameter of 25 µm. On the other hand, the metal spacer is used for glue to secure a consistent BLT for package with strict requirement in glue height. The used of spacer will eliminate the occurrence of BLT not less than the spacer diameter.

One main challenge raised is the current capability of each machine platform in bonding a small die to a higher BLT range. This paper discussed the result of evaluating different machine platforms to materialize a higher BLT given the small die setup.

2. REVIEW OF RELATED LITERATURE

A conventional assembly process flow for tapeless QFN leadframe technology is given in Fig. 2 highlighting the assembly process in focus. Important to note that assembly process flow varies with the product and the technology [1-3]. Furthermore, with new and continuous technology trends and breakthroughs, challenges in assembly manufacturing are unavoidable [4-7].

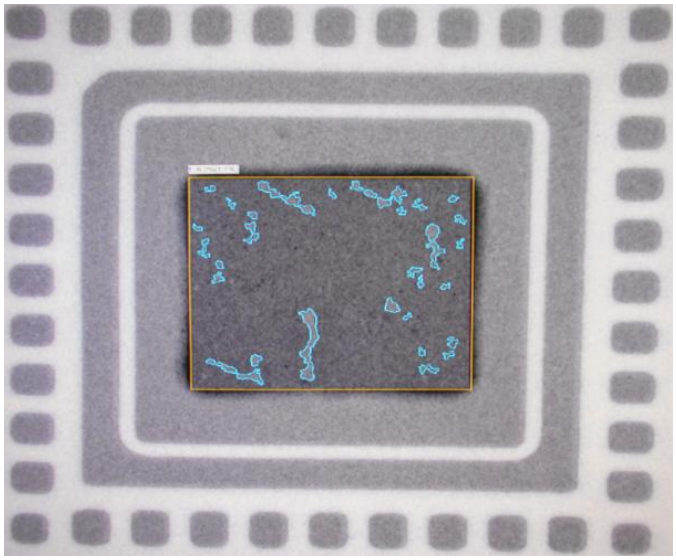

Fig. 1. X-ray image of QFN package with glue voids

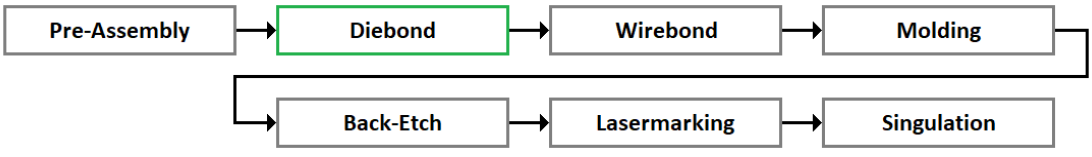

Fig. 2. Assembly process flow applicable to the package in focus

Diebonding is the process of attaching a semiconductor die either on a leadframe or in the substrate carrier. The method of attaching the die to a carrier is formed using the sequence: 1) the ejector needle ejects-up the semiconductor die from the wafer tape; 2) the rubber tip picks the die from the needle; 3) the picked die is placed on the already dispensed substrate and leadframe; 4) the bonding height is determined by the bonding parameter together with the dispense configuration. Glue diebonding uses the epoxy glue as the main adhesive to attach the die. The dispensing of glue on the pad of lead frame or substrate is done using a volumetric type dispenser. Based on the standard operating procedure, the shaped and condition of the glue is determined by the interaction of dispensing parameter, indirect material and glue type.

In recent studies, bond line thickness (BLT) has a major impact in reducing the package stress. The BLT is crucial for the coefficient of thermal expansion (CTE) mismatch between silicon die and thermal pad. A defined height of BLT is needed to act as a suitable mechanical relief since lower bond line thickness results to package delamination. BLT is being measured by the distance from the carrier die paddle to the bottom part of the silicon die as shown in Fig. 3. Normally, BLT specification rangers from 5 µm to 50 µm. BLT also have measurements that are not equal at all corners. The computation to acquire the bond line thickness of the unit given in Fig. 4 is the average thickness of the four corners of the silicon die less than the silicon die thickness.

3. METHODOLOGY

BLT was evaluated in the design of experiment (DOE) on two different diebond machine platforms. Note that BLT criteria is governed by internal specification and work instruction [8]. Machine 1 is an older version that can only meet the BLT criteria of less than 25 µm with a dispensing technology of volumetric dispense. On the other hand, Machine 2 is a new technology of another supplier that is designed to a high capability to meet a higher BLT with a pneumatic dispensing technology wherein you can control the volume of epoxy through pressure. Machine 2 is also able to produce more units per hour in glue-based packages compared to Machine 1.

The data gathering flow is described in Fig. 5. The 8" wafer is taped to protect the front side layer during back lap or wafer back grinding. The wafer will be grinded into 280 µm final die thickness. The diced wafer is transferred to diebond station for setup and optimization, then the bonded unit will be measured according to the required metrics.

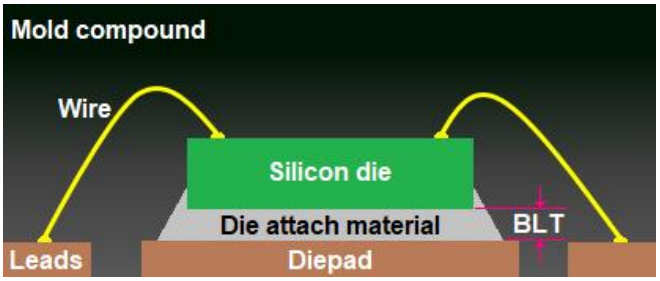

Fig. 3. QFN package cross-sectional representation

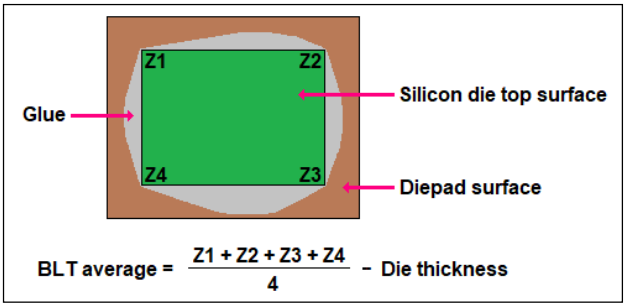

Fig. 4. Measuring BLT during data gathering

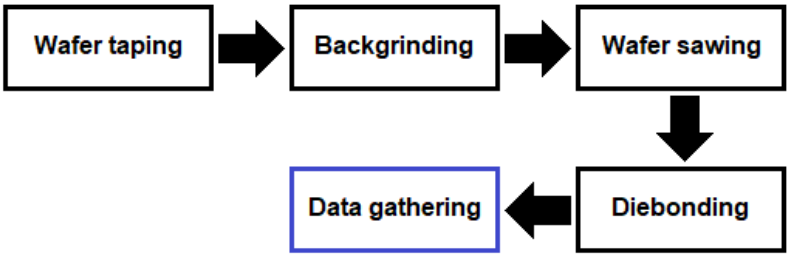

Fig. 5. Data gathering flow

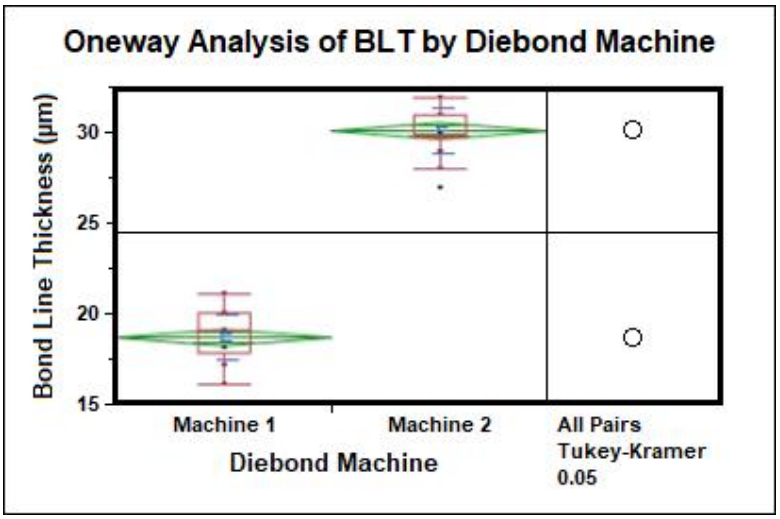

Fig. 6. Statistical analysis of BLT on two diebond machine platforms

4. RESULTS AND DISCUSSION

Bond line thickness is the height of an epoxy when bonding the silicon die on the lead frame or carrier. Using similar indirect material and dispense parameter such as epoxy shape and dispense ratio, BLT is measured along two machine platforms. Analysis of variance in Fig. 6 shows that there is a significant difference between the two machine platforms. Machine 2 platform shows significant improvement in the BLT mean, with 30.89 µm average compared to 18.25 µm of Machine 1. With this, the target BLT range could only be achieved in Machine 2 only.

5. CONCLUSION AND RECOMMENDATIONS

The paper discussed the evaluation of different machine platforms to realize a higher BLT on a small die setup. In this study, it has been shown that Machine 2 has significant improvement in the BLT performance, capable of processing BLT of more than the target of 30 µm. Note that higher BLT creates more clearance for the shrinkage of the glue, therefore, eliminating the glue voids and realizing a robust package.

For succeeding works and studies, Machine 2 platform and its configuration could be considered as a reference in handling semiconductor packages with similar requirement at diebonding process. Comparison of existing works should also be included for added analysis. Studies and learnings shared in [9-12] are helpful to improve the assembly processes particularly the diebonding process.

ACKNOWLEDGEMENT

The authors are thankful to the New Product Development & Introduction (NPD-I) team and the Management Team for the great support.

COMPETING INTERESTS

Authors have declared that no competing interests exist.

REFERENCES

1. Geng H. Semiconductor manufacturing handbook. 2nd Ed., McGraw-Hill Education, USA; 2017.
2. Harper C. Electronic packaging and interconnection handbook. 4th Ed., McGraw-Hill Education, USA; 2004.
3. Doering R, Nishi Y. Handbook of semiconductor manufacturing technology. 2nd Ed., CRC Press, USA; 2007.
4. Xian TS, Nanthakumar P. Dicing die attach challenges at multi die stack packages. 35th IEEE/CPMT International Electronics Manufacturing Technology Conference, Malaysia; 2012.
5. Liu Y, Irving S, Luk T, Kinzer D. Trends of power electronic packaging and modeling. 10th Electronics Packaging Technology Conference, Singapore; 2008.
6. Sumagpang Jr. A, Rada A. A systematic approach in optimizing critical processes of high density and high complexity new scalable device in MAT29 risk production using state-of-the-art platforms. Presented at the 22nd ASEMEP Technical Symposium, Philippines; 2012.
7. Tsukada Y, Kobayashi K, Nishimura H. Trend of semiconductor packaging, high density and low cost. 4th International Symposium on Electronic Materials and Packaging, Taiwan; 2002.
8. STMicroelectronics. Work instruction for die attach monitoring. rev. 65.0; 2019.
9. Meng LH, Hoe MC. Thermal simulation study of die attach delamination effect on tqfp package thermal resistance. 34th IEEE/CPMT International Electronic Manufacturing Technology Symposium (IEMT); 2010.
10. Graycochea Jr. E, Gomez FR, Rodriguez R. Warpage mitigation through diebond process improvement with enhanced leadframe configuration. Journal of Engineering Research and Reports. 2020;10(2).
11. Abdullah Z, Vigneswaran L, Ang A, Yuan GZ. Die attach capability on ultra thin wafer thickness for power semiconductor. 35th IEEE/CPMT International Electronics Manufacturing Technology Conference; 2012.
12. Huang HH, Wey J. Research on the high-speed pick and place device for die bonders. 8th IEEE International Conference on Control and Automation. 2010;2(2).

Peer-review history:
The peer review history for this paper can be accessed here:
http://www.sdiarticle4.com/review-history/58701